WHAT IS CLAIMED IS:

1. A dynamic logic circuit having an output and a complementary output comprising:

a first electronic switch having an input terminal coupled to a clock signal, a first terminal coupled to a positive power supply voltage and a second terminal coupled to a dynamic node of said dynamic logic circuit, wherein said dynamic node is coupled to said positive power supply voltage in response to a first logic state of a clock signal and isolated from said positive power supply voltage in response to a second logic state of said clock signal;

a logic tree having a plurality of logic inputs, a positive tree terminal coupled to said dynamic node and a negative tree terminal, wherein said positive tree terminal is coupled to said negative tree terminal in response to first logic states of said plurality of logic inputs and isolated from said negative tree terminal in response to second logic states of said plurality of logic inputs;

a second electronic switch having an input coupled to said clock signal, a first terminal coupled to said negative tree terminal and second terminal coupled to a negative power supply voltage, wherein said negative tree terminal is coupled to said negative power supply voltage in response to said second logic state of a clock signal and isolated from said positive power supply voltage in response to a first logic state of said clock signal;

a keeper circuit having a power supply terminal coupled to a positive power supply voltage, a keeper output coupled to said dynamic node, a keeper input coupled to said complementary output, wherein said keeper circuit reinforces a first logic state on said dynamic node only when said dynamic node evaluates to a logic one and said output transitions to a logic zero; and

static output logic circuitry having an input coupled to said dynamic node, a static output generating said output, an inverted static output generating said complementary output, and an enable terminal, wherein said enable terminal is coupled to said negative power supply voltage by a third electronic switch in response to said second logic state of said clock signal and by a fourth electronic switch in response to said second logic state of said complementary output.

2. The dynamic logic circuit of claim 1, wherein said keeper circuit comprises a P channel field effect transistor (PFET) having a gate terminal coupled to said complementary output, a source terminal coupled to said power supply terminal and a drain terminal coupled to said keeper output.

3. The dynamic logic circuit of claim 1, wherein said complementary output is generated by inverting said output using an inverter logic gate.

4. A logic device comprising:

a plurality of dynamic logic circuits wherein each of said dynamic logic circuits has a first electronic switch having an input terminal coupled to a clock signal, a first terminal coupled to a positive power supply voltage and a second terminal coupled to a dynamic node of said dynamic logic circuit, wherein said dynamic node is coupled to said positive power supply voltage in response to a first logic state of a clock signal and isolated from said positive power supply voltage in response to a second logic state of said clock signal, a logic tree having a plurality of logic inputs, a positive tree terminal coupled to said dynamic node and a negative tree terminal, wherein said positive tree terminal is coupled to said negative tree terminal in response to first logic states of said plurality of logic inputs and isolated from said negative tree terminal in response to second logic states of said plurality of logic inputs, a second electronic switch having an input coupled to said clock signal, a first terminal coupled to said negative tree terminal and second terminal coupled to a negative power supply voltage, wherein said negative tree terminal is coupled to said negative power supply voltage in response to said second logic state of a clock signal and isolated from said positive power supply voltage in response to a first logic state of said clock signal, a keeper circuit having a power supply terminal coupled to a positive power supply voltage, a keeper output coupled to said dynamic node, a keeper input coupled to said complementary output, wherein said keeper circuit reinforces a first logic state on said dynamic node only when said dynamic node evaluates to a logic one and said output transitions to a logic zero, and static output logic circuitry having an input coupled to said dynamic node, a static output generating said output, an inverted static output generating said complementary output, and an enable terminal, wherein said enable terminal is coupled to said negative power supply voltage by a third electronic switch in response to said second

logic state of said clock signal and by a fourth electronic switch in response to said second logic state of said complementary output.

5. The dynamic logic circuit of claim 4, wherein said keeper circuit comprises a P channel field effect transistor (PFET) having a gate terminal coupled to said complementary output, a source terminal coupled to said power supply terminal and a drain terminal coupled to said keeper output.

6. The dynamic logic circuit of claim 4, wherein said complementary output is generated by inverting said output using an inverter logic gate.

7. A data processing system comprising:

a central processing unit (CPU); and

a memory operable for communicating instructions and operand data to said CPU, wherein said CPU includes a logic system having a logic device, said logic device including a plurality of dynamic logic circuits wherein each of said dynamic logic circuits has a first electronic switch having an input terminal coupled to a clock signal, a first terminal coupled to a positive power supply voltage and a second terminal coupled to a dynamic node of said dynamic logic circuit, wherein said dynamic node is coupled to said positive power supply voltage in response to a first logic state of a clock signal and isolated from said positive power supply voltage in response to a second logic state of said clock signal, a logic tree having a plurality of logic inputs, a positive tree terminal coupled to said dynamic node and a negative tree terminal, wherein said positive tree terminal is coupled to said negative tree terminal in response to first logic states of said plurality of logic inputs and isolated from said negative tree terminal in response to second logic states of said plurality of logic inputs, a second electronic switch having an input coupled to said clock signal, a first terminal coupled to said negative tree terminal and second terminal coupled to a negative power supply voltage, wherein said negative tree terminal is coupled to said negative power supply voltage in response to said second logic state of a clock signal and is isolated from said positive power supply voltage in response to a first logic state of said clock signal, a keeper circuit having a power supply terminal coupled to a positive power supply voltage, a keeper output coupled to said dynamic node, a keeper input coupled to said complementary output, wherein said keeper circuit reinforces a first logic state on said dynamic node only when said dynamic node evaluates to a logic one and said output transitions to a logic zero, and static output logic circuitry having an input coupled to said dynamic node, a static output

generating said output, an inverted static output generating said complementary output, and an enable terminal, wherein said enable terminal is coupled to said negative power supply voltage by a third electronic switch in response to said second logic state of said clock signal and by a fourth electronic switch in response to said second logic state of said complementary output.

8. The data processing system of claim 7 wherein said keeper circuit comprises a P channel field effect transistor (PFET) having a gate terminal coupled to said complementary output, a source terminal coupled to said power supply terminal and a drain terminal coupled to said keeper output.

9. The data processing system of claim 7 wherein said complementary output is generated by inverting said output using an inverter logic gate.

10. A dynamic logic circuit having an output and a complementary output comprising:

a dynamic node;

precharge circuitry coupled to said dynamic for precharging the dynamic node to a logic one during a precharge cycle of a clock signal;

a logic tree coupled to said dynamic node for evaluating said dynamic node to a logic one or a logic zero in response to combinations of logic states of plurality of logic inputs coupled to said logic tree during an evaluation cycle of said clock signal;

static logic circuitry for latching a logic state of said dynamic node and holding said logic state during said precharge cycle of said clock signal, wherein said static logic circuitry generates said output and said complementary output; and

a keeper circuit having a power supply terminal coupled to a power supply voltage, a keeper input coupled to said complementary output and a keeper output coupled to said dynamic node, wherein said keeper output reinforces a first logic state of said dynamic node only when said dynamic node evaluates to a logic one and said output transitions to a logic zero.

11. The dynamic logic circuit of claim 10, wherein said keeper circuit comprises a P channel field effect transistor (PFET) having a gate terminal coupled to said complementary output, a source terminal coupled to said power supply terminal and a drain terminal coupled to said keeper output.